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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,467	11/12/2003	Arvind Reddy Aemireddy	AEMIREDDY 1	6748

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EXAMINER	
KAPLAN, HAL IRA	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,467	AEMIREDDY, ARVIND REDDY	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,10,12 and 14* is/are rejected.

7)☒ Claim(s) *4-9,11,13 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Paragraph 2, line 6 and paragraph 3, line 1 contain the phrase "output stage 100". It appears this should be "output stage 101". Paragraph 12, line 11 contains the phrase "4 volt". It appears this should be "4 volts". Paragraph 13, line 5 contains the symbol "$V_{threshold}$". This is not defined in the specification. Paragraph 26, lines 6 and 8 contain the phrase "output pad 207". It appears this should be "output pad 203". Paragraph 27, line 2 contains the phrase "that voltage". It appears this should be "the voltage". Paragraph 27, line 3 contains the phrase "which will cause". It appears this should be "will cause". paragraph 28, line 12 contains the phrase "transistor M3". It appears this should be "transistor M9". Paragraph 34, line 1 contains the phrase "bias voltages". It appears this should be "bias voltage".

Appropriate correction is required.

2. The disclosure is objected to under 37 CFR 1.71(a) because it is not sufficiently enabling.

The device labeled "207" in Figures 2 and 4 is identified as a multiplexer in paragraph 25, line 2, paragraph 31, line 2, and both Figures; and as a demultiplexer everywhere else throughout the specification. It is not completely clear whether this is a multiplexer or a demultiplexer. One of ordinary skill in the art would have to know which part to use in order to make and/or use the invention.

In addition, it is not clear whether transistors M1, M2, M4, M6, M7, M9, and M10 are NMOS or PMOS.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 100 in Figure 1 (see paragraph 2, line 6 and paragraph 3, line 1) and 403 in Figure 4 (see paragraph 29, line 2).

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 206 in Figure 2. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 10, 13, 14, and 17 are objected to because of the following informalities: Claim 10 lines 3-4, the phrase "the lower voltage driver" lacks proper antecedent basis.

Claim 10 line 12, the phrase "the first node" lacks proper antecedent basis. Claim 10 line 13, the phrase "the lower voltage rail" lacks proper antecedent basis. Claim 13, line 7 contains the word "comprises". It appears this should be "comprising". Claim 14 line 14, the phrase "the first node" lacks proper antecedent basis. Claim 17, line 4 contains the word "further". It appears this should be "fourth". Claim 17 lines 9 and 10, the phrase "said first node" lacks proper antecedent basis. Appropriate correction is required.

6. Claims 2, 7, 12, and 16 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

As to claims 2, 12, and 16, the comparator of claim 1, in order to be able to detect when a voltage on the first node exceeds the voltage of the lower voltage rail, must have a first input coupled to the first node and a second input coupled to the lower voltage rail. Claim 1 recites the output being coupled to the control terminal of the second transistor.

As to claims 7, 12, and 16, the comparator by definition outputs a first voltage level when the voltage at its inverting input is less than the voltage at its noninverting input, and a second voltage level when the voltage at its inverting input is greater than the voltage at its noninverting input.

Double Patenting

7. Applicant is advised that should claim 2 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

8. Claim 11 objected to under 37 CFR 1.75 as being a substantial duplicate of claim 6. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-3, 10, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US patent application publication of Vulih et al. (2004/0140719) in view of the US patent application publication of Kamiya (2002/0167771).

As to claims 1, 10, and 14, Vulih, drawn to a smooth voltage regulation transition circuit having fast recovery, teaches, in Figure 1, a circuit read on the claimed circuit, comprising a lower voltage driver (11), a higher voltage driver (14), and an input signal source (DLA), wherein the lower voltage driver includes an output stage having a first transistor (17) having a first current flow terminal coupled to a lower voltage rail (11) and a second current flow terminal coupled to drive a first node (15) (see paragraph 19, lines 2-4 and 7-10, and paragraph 20, lines 1-18). Vulih does not disclose a second transistor having a first current flow terminal coupled to the second current flow terminal of the first transistor, or a comparator.

Kamiya, drawn to a countercurrent prevention circuit, teaches, in Figure 2, a transistor (3) having a first current flow terminal (1) and a second current flow terminal (2), and further having a control terminal (see paragraph 20, lines 1-15 and Figure 2); and a comparator (5) coupled to detect when a voltage on a first node (2) exceeds the voltage of a lower voltage rail (1), the comparator (5) having an output coupled to the control terminal of the second transistor and configured to turn the second transistor off if the voltage on the first node exceeds the voltage of the lower voltage rail (see paragraph 21, lines 8-12). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to connect the circuits of Kamiya and Vulih such that the

lower voltage rail (1) of Kamiya is connected to the second current flow terminal of the first transistor (17) of Vulih and the first node (2) of Kamiya is connected to terminal 15 of Vulih (the circuit of Kamiya is in series between transistor 17 of Vulih and node 15, and the output device of the circuit of Kamiya is the higher voltage driver (14) of Vulih), in order to prevent the flow of a countercurrent from the higher voltage driver (14) of Vulih into the lower voltage driver (11).

As to claim 2, in the circuit of Vulih in view of Kamiya, the comparator (5 in Kamiya) has a first input (a) coupled to the first node (15 in Vulih), a second input (b) coupled to the lower voltage rail (11 in Vulih) and an output coupled to the control terminal of the second transistor (3 in Kamiya).

As to claim 3, the circuit of Vulih in view of Kamiya is constructed of CMOS components (17 of Vulih and 3 of Kamiya).

As to claim 12, the comparator of Kamiya is configured to output a first voltage level when the voltage on the output node (2) is less than the voltage of the input node (1) and to output a second voltage level when the voltage on the output node (2) is greater than the voltage of the input node (1).

Allowable Subject Matter

12. Claims 4-6, 8, 9, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

Claims 4-6, 8, 9, and 15 contain allowable subject matter because none of the prior art teaches or discloses a diode clamp coupled between the control terminal and the first current flow terminal of the second transistor, in combination with the remaining claimed features.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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